

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

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U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

TUP	U.S. Patent Application Serial Number 09/466,934, Filed December 20, 1999 Allowed 8/12/02
TUP	U.S. Patent Application Serial Number 09/639,953, Filed August 17, 2000 US Pat. 6,495,898
TUP	U.S. Patent Application Serial Number 09/677,881, Filed October 3, 2000 US Pat. 6,455,894
TUP	Hirano, et al., "Bulk-Layout-Compatible 0.18 μ m SOI-COS Technology Using Body-Fixed Partial Trench Isolation (PTI)" Proceedings of 1999 IEEE International SOI Conference, October 1999, pages, 131 - 132
TUP	Maeda, et al., "Analysis of Delay Time Instability According to the Operating Frequency in Field Shield Isolated SOI Circuits" Proceeding of IEEE Transactions of Electron Devices, Vol. 45, No.7, July 1998, pages 1479 - 1486

EXAMINER



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